Sync4K™ Video Synchronizer

- **Per channel DisplayPort resolutions up to 4096x2400, including UHD (3840x2160)**
- **Pixel rates to 600 MPixels/sec (2560x1600@120Hz, 3840x2160@60Hz)**
- **Order configuration is from 1 to 5 synchronizing channels**
- **Inter-channel and inter-box synchronization to support synchronized outputs**
- **Pre-programmed EDID on each input, with common high resolution timings**
- **1U rack-mount unit, pre-stored settings applied at power up**

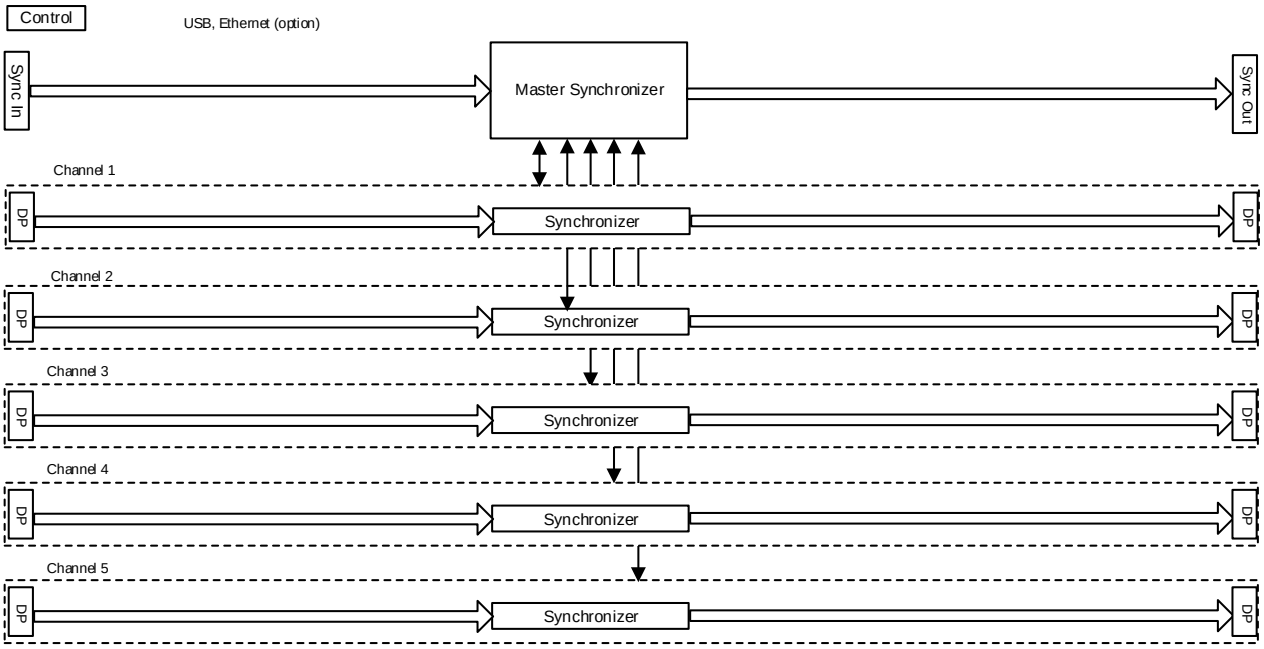

Figure 1: Sync4K block diagram (shown as DP configuration)

Synchronizing the video timings of multiple graphic cards may be required for multi-monitor or multi-projector applications. True video genlocked operation is not available with most graphics cards, and those that support genlocking are often expensive or lacking in other features. To overcome this issue, specialized software and hardware implementations will "soft sync" the video frames across otherwise independent computers and graphics cards. "Soft sync" is implemented by closed loop modifications of the video timing (ex: adding or subtracting lines) to keep the outgoing Vertical Sync (VS) within an acceptable range of the master timing's VS. These real-time modifications result in varying frame times, also known as frame jitter.

Downstream devices may not synchronize properly to the soft sync video due to the frame jitter within the video. For these situations, the Sync4K, as shown in Figure 1 above, can convert 1 to 5 soft-sync inputs into stable video, genlocked to a master timing. The Master timing is auto-selected as the "SYNC INPUT", if present. Otherwise the master timing is assumed to be Channel 1.

The diagram below depicts a typical scenario using Sync4K:

- Channel #1input timing, to be selected as the Master Timing
- Soft-sync Channel #2 input timing, that is currently "trailing" the Master Timing by 20 lines
- Soft-sync Channel #3 input timing, that is currently "leading" the Master Timing by 20 lines
- Synchronized output timing for all channels
- The output timing is pre-programmed to a 22 line delay.

The diagram is referenced in timing discussions on the ensuing pages, especially to understand timing constraints.

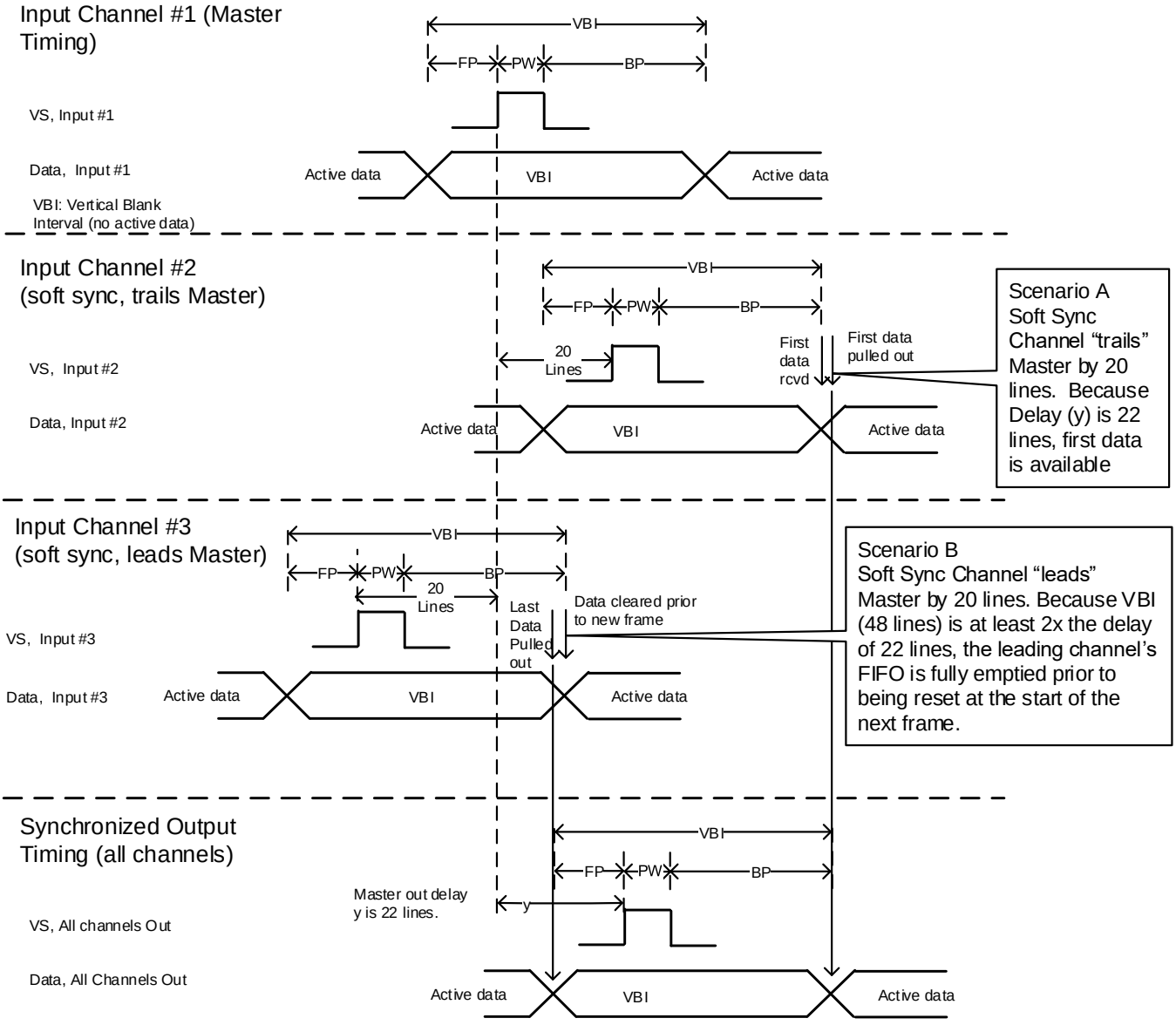

Figure 2 Timing Constraints for Sync4K

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Sync4K Video Synchronizer

The Sync4K is configured with 1 to 5 channels (referred to as synchronizing channels). Each synchronizing channel is synchronized to a master timing, which is automatically selected to be either Input 1 or the Sync Input. The first box in an installation will typically use Input 1 as the master timing, allowing up to 4 additional channels to be synchronized to it. The Sync Output sends the master timing to a downstream Sync4K Video Synchronizer to allow more channels to be synced to the master video timing.

The Sync4K re-times soft synced inputs into a stable output with a fixed frame time, locked to the master video timing with a programmable line delay (y). To avoid video artifacts, the input vertical syncs of all slave channels must be synchronized to within typically +/- 150 usecs of the master video vertical sync. (see section entitled Soft sync Constraint Analysis).

Each channel employs a FIFO memory to support channel synchronization. The input frame time typically varies by an integer # of lines during the vertical front porch. Periodic, standard video is then "pulled" from the FIFO per the master timing, delayed by the programmable line delay (y).

The Sync4K is designed to require minimal programming. All parameters have pre-programmed default values. The OneSync™ configuration utility allows the user to program parameters (such as line delay, y).

Resolutions: All channels are assumed to be the same resolution. A future option (:TG) allows a slave channel to be a different timing than the master channel.

Sync4K Features

- Synchronizes multiple channels to a master sync source
- Multiple Sync4K's can be "daisy-chained", for applications requiring more than 5 channels
- I/O resolutions up to 4kx2K/60 Hz.
- Remote interface for both initial configuration and operational control via USB or optional Ethernet
- "Active EDID" can be either the most recently connected downstream EDID, or a pre-programmed EDID
- "No video" modes:
    - In the absence of a valid master timing, the slave channels enter pass-through mode (If the master timing was from Channel 1, then Channel 1 output and Sync output are inactive)
      Note: Only stable timing is passed through. Unstable timing is not compatible with Sync4K transmitters.
    - In the absence of video input for a slave channel, the slave channel outputs a pre-programmed RGB color per the delayed master timing.

Soft sync Constraint Analysis

The Sync4K requires inputs to be synchronized to within certain constraints. Two Sync4K design items dictate constraints on the incoming soft synced channels. These design items are as follows:

1. Each synchronizing channel has 200,000 pixels of FIFO depth,
2. A synchronizing channel's FIFO is "cleared" each frame, at the very end of the Vertical Blanking interval (just prior to receiving Line 1 Pixel 1 of active video). Thus all pixels from the previous frame must be emptied by that point or they will be cleared.

Scenario A: Because soft-synced channels tend to vary +/- x lines from the master timing, the programmed line delay y must be greater than x so that the new pixel data in a "trailing" slave channel has arrived at FIFO inputs prior to outputting that pixel data from the FIFO. See "Scenario A" in Figure 2.

Scenario B: The Vertical Blanking Interval (VBI) must be greater than 2y. This allows sufficient time for the "leading" slave channel's pixel data to be fully emptied of the previous frame, prior to clearing the FIFO at the start of a new incoming frame. See "Scenario B" in Figure 2.

Example: Each specific configuration will require its own analysis, but for this discussion we assume the master timing and soft synced channels are 3840x2160 @ 60 Hz (UHD).

Design item 1 equates to a line buffer size of:
200,000 pixels / (3840 pixels/line) = 52 lines.
Thus up to 52 lines can be stored. In Figure 2, a synchronizing channel that leads the master by 20 lines and then has an additional 22 lines of delay, will need 42 lines of storage. This is within the constraint of 52 lines.

Design item 2: In Figure 2, we see that the VBI (48 lines) is long enough (> 2y) such that all data from the previous frame is pulled out prior to the clearing function at the start of a new frame. Standard UHD has a VBI = 90 lines, more than sufficient to meet this constraint.

Output Video Timing

The output timing for any synchronizing channel is identical to the master timing, but delayed by y lines. **A future option (:TG) will allow a slave channel to be a different timing than the master timing. In this case, the desired timing is derived from the "active EDID" (either a downstream EDID or a pre-programmed EDID).**

Master video timing is automatically selected from the Sync Input or Input 1. The Sync input can only be connected to a Sync output from an upstream Sync4K device.

Option ":TG"- Different slave timing

A future option (:TG) will support a slave timing different than the master timing. In this case, the output slave timing is defined by the "active EDID". The output clock is derived from the repeater (master) timing and desired output timing as follows:

VRtotal	= Total lines per frame in Repeater Video
HRtotal	= Total clocks per line in Repeater Video
PclkR	= Frequency of the Repeater Clock
VOtotal	= Total lines per frame in Output Video
HOtotal	= Total clocks per line in Output Video
PclkO	= Frequency of the Output Clock

Due to gen-locking:

Frame Time, Repeater	= Frame Time, Output
VRtotal*HRtotal/PclkR	= VOtotal*HOtotal/PclkO
PclkO	= PclkR * (VOtotal*HOtotal) / (VRtotal*HRtotal)

Other Features

EDID: The active EDID, available to the video source via the DP aux channel, can be either a) a pre-programmed value, or b) the EDID read from a downstream device.

A Hot Plug Detection on a Sync4K output initiates a new DisplayPort Link training session and the reading of the downstream EDID for that channel.

The user selects whether the "active EDID" is:

a. updated to the "downstream" device's EDID or
b. remains a pre-programmed EDID on each input channel.

If "a" then a change to the "Active EDID" results in a "Hot Plug Detect" event to the upstream video source.

"No Video" modes: When valid input is not detected on Channel 1 or Sync Input, then Channel 1 output and Sync Output are inactive and the slave channels automatically enter "pass-through" mode, where video is passed through the slave channel without synchronization. **Only stable timing is passed through. Unstable timing is not compatible with Sync4K transmitters.**

In the absence of slave video input, the slave output runs per the delayed master timing, but with a pre-programmed RGB color.

With future option (:TG), any channel without valid input ***and*** without the presence of master timing will enter a free running mode with timing based on the "active EDID".

OneSync™ Configuration Application

OneSync is a Windows 10 application (see Figure 3) to configure the Sync4K for an installation application. Typical set up parameters include:

Line Delay: "y", Programmed globally. The # of master timing lines to delay the synchronized outputs from the input master timing.

Active EDID mode: Programmed per channel. Determines whether the active EDID, visible by the video source, is populated by a programmed EDID file, or by the connected downstream device.

Pass-through Video: Programmed per channel. Allows the video from any input channel to be passed through as is (including timing), rather than synced to master timing.

Ignore Video: Programmed per channel. Replaces incoming pixel data with a hard-coded color, unique per channel.

In addition to parameter setup, the OneSync application also indicates the following status:

- Master Timing Source (Chan 1, Sync Input, absent)
- Input Video Present (per channel)

OneSync supports the update of the pre-programmed EDID for each channel.

OneSync supports the update of all firmware in the Sync4K.

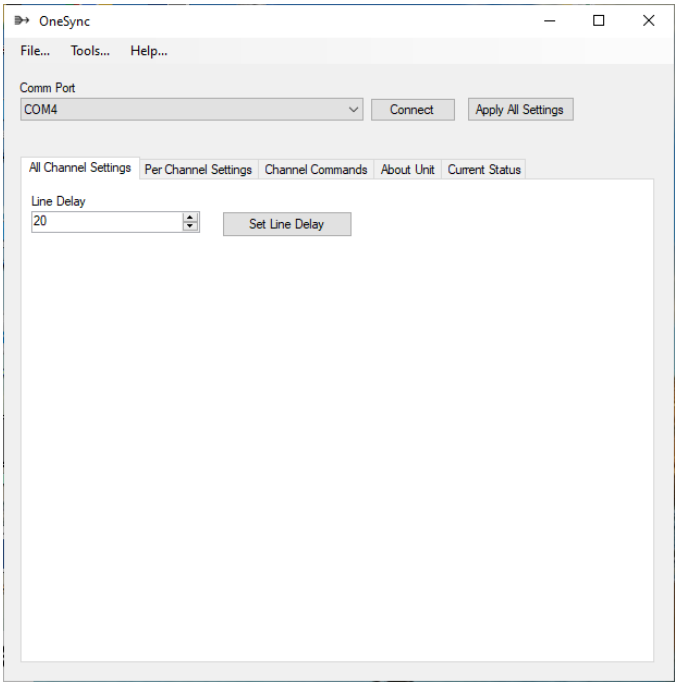

Figure 3 OneSync Configuration Application

Selecting the line delay "y": The user must know the incoming VBI. **It is assumed the VBI will vary by only +/- 1 line from this value.** Westar recommends the following methodology in picking line delay "y":

1. Select a line delay y = VBI/2 – 1
   This will handle a phase variation of x lines = +/- (y-1)
2. Ensure the FIFO is big enough as follows:
   [x max leading lines + y delay lines] * Hres (pixels/line) <= 200,000 pixels (FIFO depth)

Please call Westar for assistance.

Sync4K Specifications

Figure 4 summarizes the Sync4K specifications.

Input / Output Specifications (per channel)		
	Video Type	DisplayPort 1.2
	Pixel Rate	Up to 600 MPixels/sec
	Standard resolutions	Up to 2560x1600 at 120 Hz, 4096x2400 at 60 Hz
Electro Mechanical		
	Input Power	IEC Connector, 100-240 VAC, 47-63 Hz, 100 Watts Maximum Input Power
	Control	USB 2.0, Ethernet (option)
	Size	19"W x 14.5"D x 1.75"H (1U rackmount)
	Weight	Less than 6 lbs.
FIFO storage		200,000 pixels of FIFO depth per channel
Functional		
	Color Depth	Up to 10 bits per color I/O.
	Specialty Features	Programmable EDID for each input channel
		If no Sync Input or Channel 1 (master timing), slave channel enters pass-through mode. Only stable timings are passed through
		If no slave channel input, channel outputs a RGB color per master timing
Warranty		One year
Each Sync4K delivery includes:		Sync4K unit configured with I/O channels as ordered, rack-mount ears, IEC power cable with US plug, USB cable, and a CD containing: OneSync Utility Software Sync4K Documentation

Figure 4 Sync4K Specifications

Figure 5 Sync4K-DP5 rear panel

Ordering Info / Notes:

The Sync4K is ordered as follows:

Sync4K-DPx, where

x is the number of I/O channels
DP indicates DisplayPort I/O
:E Ethernet option
:TG supports a per channel timing generator necessary for both free running mode, and for timing generation for slave channels that are a different timing than the master channel

Examples: Sync4K-DP3
Sync4K-DP5 :E
Sync4K-DP5 :E :TG